

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device that reduces the time for conducting a multiple word line selection test and operates stably. The semiconductor memory device includes memory cell blocks, row decoders, sense amps, block control circuits, and sense amp drive circuits. Each block control circuit generates a reset signal. The reset signal is used to select the word lines with the row decoders at timings that differ between the blocks. Each block control circuit provides the reset signal to the associated row decoder. The block control circuit also provides the reset signal to the associated sense amp drive circuit so that the sense amps are inactivated at timings that differ between the blocks.